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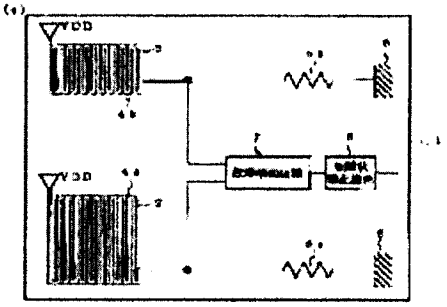
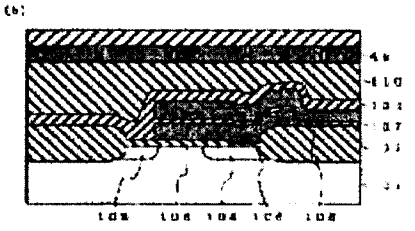
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To electrically detect a state where light is being applied due to the crack of a shielding layer, by setting a protection wiring layer so that a continuous wiring is laid at a specific region on a semiconductor chip at a small gap.

SOLUTION: Protection wiring layers 4a and 4b are formed via interlayer insulation layers 109 and 110. The protection wiring layers 4a and 4b are formed so that a desired region on an EEPROM 2 and a random circuit 3 can be nearly covered without causing adjacently arranged wirings to contact each other. No light enters below the covered region. A failure detection circuit 7 is connected from a part on the EEPROM 2 of the protection wiring layer 4a to a resistor 5a. When the protection wiring layers 4a and 4b are cracked, a failure detection signal is outputted from the failure detection circuit 7 and is stored in a failure state storage part 8, thus electrically detecting a state where light is applied due to the crack of a shielding layer.





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CLAIMS

[Claim(s)]
[Claim 1]A protection wiring layer which comprised material which a power supply is supplied when it arranges on a semiconductor chip in which an integrated circuit was formed, and said semiconductor chip and said integrated circuit operates, and intercepts light, and has conductivity, Where said protection wiring layer is formed in a desired state, detect voltage currently impressed to said protection wiring layer, and the voltage is provided with a failure detection circuit which detects the state of differing from a time of voltage by said power supply being impressed to said protection wiring layer, as an abnormal signal, and it said protection wiring layer, A semiconductor device, wherein continuous wiring is in a state with which a predetermined region on said semiconductor chip was covered at a detailed interval.
[Claim 2]A semiconductor device provided with a failed state storage parts store which memorizes an abnormal signal which said failure detection circuit detected in the semiconductor device according to claim 1.
[Claim 3]A semiconductor device if an abnormal signal is detected by said failure detection circuit in the semiconductor device according to claim 1, wherein operation of said integrated circuit will be suspended.
[Claim 4]A semiconductor device if an abnormal signal is memorized by said failed state storage parts store in the semiconductor device according to claim 2, wherein operation of said integrated circuit will be suspended.
[Claim 5]A semiconductor device, wherein directions which arrange said protection wiring layer via an insulator layer, and are provided with it more than two-layer in the semiconductor device according to claim 1 and to which wiring in each layer extends differ mutually.
[Claim 6]A semiconductor device, wherein it has electrically nonvolatile memory in which writing and elimination are possible into said integrated circuit in a semiconductor device given in Claims 1-5 any 1 clause.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the semiconductor device which consists of a semiconductor chip which equipped the integrated circuit upper part with the protection wiring layer, for example.
[0002]
[Description of the Prior Art]For example, as an external storage in the portable computer which thought the communication function as important, the nonvolatile memory (EEPROM) in which writing and elimination are possible is used increasingly electrically now. The fundamental cell of this EEPROM has composition as shown in drawing 3, for example. That is, the source 303 and the drain 304 are arranged to the field divided by the field oxide 302 on the p semiconductor substrate 301 of type. And it has the composition that the floating gate 306 electrically insulated from the circumference was formed via the gate dielectric film 305 on it, and the control gate 308 was formed via the insulator layer 307 on it. The floating gate 306 and the control gate 308 comprise polysilicon in which the impurity was introduced into high concentration.
[0003]In the above composition, a part is thin to about 10 nm, and the gate dielectric film 305 between the floating gate 306 and the drain 304 is formed.
If positive voltage sufficiently higher than the drain 304 is applied to the control gate 308, an electron will go into the floating gate 306 from the drain 304.
This is considered as elimination. If the polarity of the voltage applied to the control gate 308 is changed to the above thing, it will escape from the electron included in the floating gate 306 to the drain 304. This is considered as writing. The electron flow which passes the thin gate dielectric film 305 mentioned above is based on tunneling.
[0004]And a transistor is turned on when the electron is not contained in the floating gate. On the other hand, when many electrons are contained in the floating gate, with the negative charge of the electron in a floating gate, a channel becomes is hard to be induced between source drains, and a transistor is not turned on. These two on-off states

correspond to "0" and "1."
[0005]As shown above, EEPROM has the advantage that writing of each memory cell and elimination can be performed electrically. However, this EEPROM has the problem that the stored data will be automatically eliminated by the exposure of ultraviolet rays. For this reason, he has a light-shielding film on an EEPROM cell, and is trying to intercept penetration of the ultraviolet rays leading to elimination of data in the former, as shown in document (JP,H5-38915,U). Drawing 4 is a top view showing one in the state where this light-shielding film has been arranged.
He is trying to arrange the ultraviolet-rays filter layer 403 on it for every memory cell in the field of EEPROM402 on the semiconductor chip 401 in which the integrated circuit was formed.

[0006]
[Problem to be solved by the invention]However, since it was not recognized only by forming the ultraviolet-rays filter layer like before until the state carries out exterior observation when the ultraviolet-rays filter layer is damaged by a certain cause, there was a problem that the reliability of the data memorized could not be guaranteed. That is, when the ultraviolet-rays filter layer is damaged, ultraviolet rays will be irradiated by the EEPROM cell from the breakage field, and the data currently held will be destroyed. Here, the breakage state of an ultraviolet-rays filter layer is detectable if exterior observation of the semiconductor chip provided with the integrated circuit constituted from an EEPROM is carried out. However, when the semiconductor chip is built into the data communication equipment etc., the state of EEPROM always cannot observe from outside in many cases.
[0007]In such a case, even if breakage has arisen in the ultraviolet-rays filter layer, therefore data is destroyed, the state cannot be detected but the Data Processing Division using unusual data will be performed. Since the ultraviolet-rays filter layer is arranged on the word line etc., it may have caused the breakage and the open circuit of upper wiring which constitute EEPROM by the breakage. Such a state cannot be detected by an above-mentioned thing, either, but becomes the cause of causing malfunction of the apparatus using this semiconductor chip.
[0008]In the semiconductor chip in which the filter layer which this invention is made in order to cancel the above problems, and intercepts penetration of lights, such as ultraviolet rays, is formed, It aims at enabling it to detect electrically the state where light was irradiated by breakage of the filter layer by the integrated circuit which constitutes the semiconductor chip.
[0009]
[Means for solving problem]The semiconductor device of this invention comprises:
The semiconductor chip in which the integrated circuit was formed.
The protection wiring layer which comprised material which a power supply is supplied, intercepts light and has conductivity when it arranges on the semiconductor chip and the

integrated circuit operates.
The failure detection circuit which detects the voltage currently impressed to the protection wiring layer, and detects the state of differing from the time of the voltage by a power supply being impressed to the protection wiring layer where the voltage is formed in the state of a request of a protection wiring layer, as an abnormal signal.
and the wiring which is **(ing) the protection wiring layer -- the predetermined region on a semiconductor chip -- a ream -- it was made to be in the state where it was covered at the detailed interval Since it constituted in this way, penetration of the light to an integrated circuit is interrupted by the protection wiring layer.
[0010]
[Mode for carrying out the invention]This embodiment of the invention is described with reference to figures below. Drawing 1 is a block diagram showing the composition of the semiconductor device in a 1st embodiment of this invention. As shown in drawing 1 (a), on the semiconductor chip 1, EEPROM2 and the random circuit 3 are formed as an integrated circuit. And he is trying to form those protection wiring layers 4a and 4b that are EEPROM2 and consist of aluminum on the random circuit 3, for example in the semiconductor device of this embodiment. The material which constitutes the protection wiring layers 4a and 4b is not restricted to aluminum, and it may be made to use other metallic materials, such as Cu and Ti. Namely, the protection wiring layers 4a and 4b intercept light, and should just have conductivity.
[0011]Drawing 1 (b) shows the section in a part of EEPROM2 of drawing 1. If the outline composition of EEPROM is explained using this drawing 1 (b), the source 103 and the drain 104 are first arranged to the field divided by the field oxide 102 on the p semiconductor substrate 101 of type. And it has the composition that the floating gate 106 electrically insulated from the circumference was formed via the gate dielectric film 105 on it, and the control gate 108 was formed via the insulator layer 107 on it. The floating gate 106 and the control gate 108 comprise polysilicon in which the impurity was introduced into high concentration.
[0012]In the above composition, some gate dielectric film 105 between the floating gate 106 and the drain 104 is thinly formed in about 10 nm. And if positive voltage sufficiently higher than the drain 104 is applied to the control gate 108, in a field of the thin gate dielectric film 105, an electron will go into the floating gate 106 from the drain 104. This is eliminated. If the polarity of voltage applied to the control gate 108 is changed to the above thing, it will escape from an electron included in the floating gate 106 to the drain 104. This becomes writing.
[0013]And the protection wiring layers 4a and 4b were formed via the interlayer insulation film 109,110 on this. One end was connected to the power supply VDD, respectively, and these protection wiring layers 4a and 4b have connected the other end to the grounding 6 via the resistance 5a and 5b, as shown in drawing 1 (a). And without the wiring arranged next contacting, these protection wiring layers 4a and 4b are formed so that a field

considered as a request on EEPROM2 and the random circuit 3 may be covered mostly. For this reason, it is in the state where light hardly enters under a covered field. For example, the failure detection circuit 7 has connected from a portion on EEPROM2 of the protection wiring layer 4a before the resistance 5a. This is the same also in the protection wiring layer 4b. And an output of the failure detection circuit 7 is memorized by the failed state storage parts store 8.

[0014]Since it has composition shown above, while the semiconductor device is operating to the protection wiring layers 4a and 4b, it is always in the state where the power supply VDD was impressed to them, and the potential is maintained at the potential (normal potential) specified by the resistance 5a and 5b. For this reason, for example, if an open circuit arises in the protection wiring layer 4a, the potential between that open-circuit portion and resistance 5a will become what has the different normal potential mentioned above (unusual potential). Similarly, if an open circuit arises in the protection wiring layer 4b, the potential between the open-circuit portion and resistance 5b will turn into normal potential mentioned above with difference unusual potential. And in the failure detection circuit 7, when these potential is supervised and at least the one either detects unusual potential (abnormal signal), failure detection signals are outputted. And the failure detection signals outputted from this failure detection circuit 7 are memorized by the failed state storage parts store 8.

[0015]Therefore, according to this embodiment, EEPROM2 and the random circuit 3 will be protected from an optical exposure by the protection wiring layers 4a and 4b. For this reason, for example, in EEPROM2, it becomes possible to protect the data currently recorded from elimination by optical exposure. And according to this embodiment, breakage arises in the protection wiring layers 4a and 4b, and even if it does not perform exterior observation that abnormalities occurred to the data currently recorded by the optical exposure from this damaged part, it can detect. That is, if breakage arises in the protection wiring layers 4a and 4b, as mentioned above, failure detection signals will be outputted from the failure detection circuit 7, and this will be memorized by the failed state storage parts store 8. Therefore, if the memory content of this failed state storage parts store 8 is checked, it will become possible to detect that data abnormality.

[0016]The failure detection circuit 7 and the failed state storage parts store 8 which were mentioned above are good also as composition shown below. For example, it constitutes from an inverting circuit which reverses two input signals for the failure detection circuit 7, respectively, and an OR circuit which takes those "OR", and may be made to constitute the failed state storage parts store 8 from a flip-flop. With constituting in this way, if there is no open circuit in the protection wiring layers 4a and 4b, two inputs of an OR circuit will serve as "Low", and a flip-flop will also serve as the "Low" level. on the other hand, the protection wiring layers 4a and 4b -- if either has an open circuit, one of two inputs of an OR circuit will serve as "High", a flip-flop will also serve as the "High" level, and this will be held.

[0017]and this flip-flop -- "Low" and "High" -- it can be checked by checking whether it is in

which state whether abnormalities have occurred in the semiconductor device of drawing 1. When this flip-flop is the "High" level, it may prevent from operating the semiconductor device of drawing 1. A reset circuit is connected to the output destination change of the flip-flop, and when a flip-flop is the "High" level, it may be made to be in the state where the semiconductor device of drawing 1 always performs initializing operation. Namely, when abnormalities have occurred in the semiconductor device, it may be made to change into the state which cannot use the semiconductor device. By doing in this way, the equipment failure etc. to which this semiconductor device is connected can be prevented.

[0018]By the way, although he is trying for each wiring which constitutes a protection wiring layer to form in a uniform direction for a long time, it does not restrict to this and may be made to form the protection wiring layer 201 made spiral in the above-mentioned embodiment, as shown in drawing 2 (a). As mentioned above, it is necessary to connect a power supply to one end of this protection wiring layer 201, and to connect the other end to a failure detection circuit here. Therefore, as shown in drawing 2 (a), the protection wiring layer 201 needs to pull out the wiring 202 currently formed via the insulator layer from the central part.

[0019]As shown in drawing 2 (b), the protection wiring layer 203 may have two-layer composition arranged so that the direction of wiring may go direct. In this case, this protection wiring layer 203 has the structure where the protection wiring layer 203a arranged in a lower layer and the protection wiring layer 203b arranged via an insulator layer in that upper layer were connected via the contact 203c. Thus, with constituting the protection wiring layer 203, it becomes possible to improve a light sheilding more.

[0020]

[Effect of the Invention]The semiconductor chip in which the integrated circuit was formed in this invention as explained above, The protection wiring layer which comprised material which a power supply is supplied when it arranges on the semiconductor chip and the integrated circuit operates, and intercepts light, and has conductivity, It has a failure detection circuit which detects the voltage currently impressed to the protection wiring layer, and detects the state of differing from the time of the voltage by a power supply being impressed to the protection wiring layer where the voltage is formed in the state of a request of a protection wiring layer, as an abnormal signal, It was made for the protection wiring layer to be in the state where the predetermined region on a semiconductor chip was covered with continuous wiring at the detailed interval. That is, according to this invention, penetration of the light to an integrated circuit has composition interrupted by the protection wiring layer. Therefore, according to this invention, since it will be detected in a failure detection circuit if a protection wiring layer is damaged, the state where light was irradiated by breakage of the protection wiring layer to the integrated circuit etc. can detect electrically.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the semiconductor device in a 1st embodiment of this invention.
[Drawing 2]It is a top view showing the composition of a protection wiring layer.
[Drawing 3]It is a sectional view showing a part of fundamental cell of EEPROM.
[Drawing 4]It is a top view showing one in the state where the light-shielding film has been arranged on EEPROM.
[Explanations of letters or numerals]
101 [-- A drain, 105 / -- Gate dielectric film, 106 / -- A floating gate, 107 / -- An insulator layer, 108 / -- A control gate, 109,110 / -- Interlayer insulation film.] -- A semiconductor substrate, 102 -- Field oxide, 103 -- A source, 104

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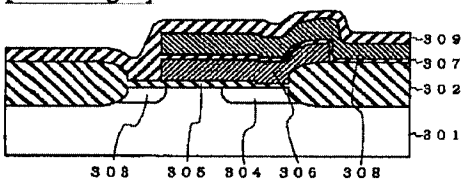
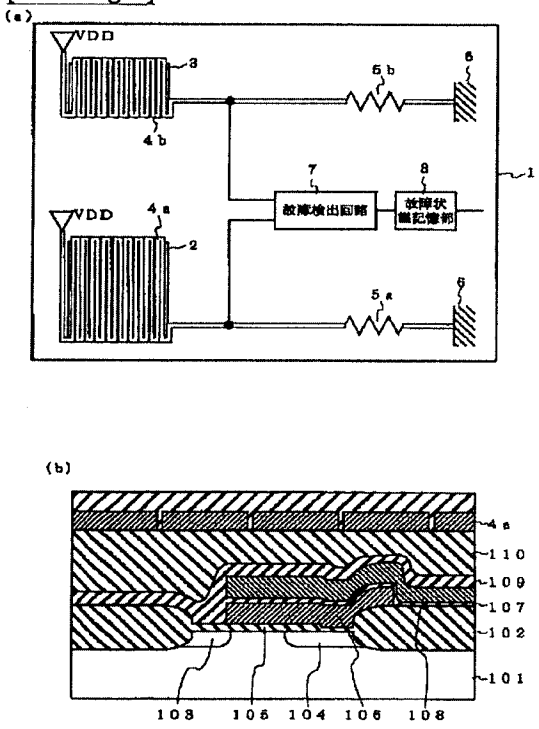
DRAWINGS

[Drawing 3]

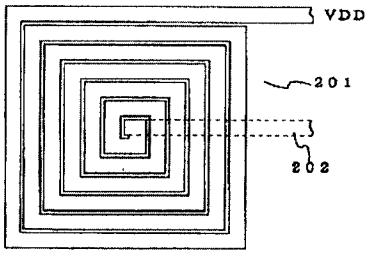


[Drawing 1]



[Drawing 2]

(a)



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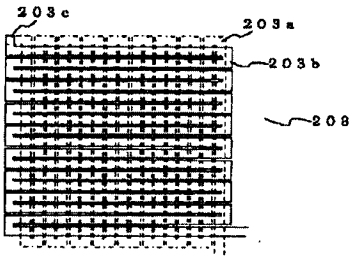
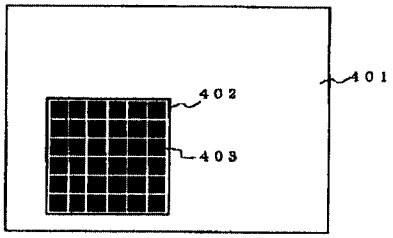


[Drawing 4]



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